(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 536 696 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **92117036.1**

(51) Int. Cl.5: **G11C 16/06**

(22) Date of filing: **06.10.92**

(30) Priority: **07.10.91 JP 259471/91**

(43) Date of publication of application:
14.04.93 Bulletin 93/15

(84) Designated Contracting States:
DE FR GB

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(54) Semiconductor memory device.

(57) A NOR operation is performed on the address bits by bits by a NOR circuit (31), and when the final address in a page is detected from the result of the NOR operation by a final address detection circuit (32), a program starting circuit (33) executes data writing to a memory cell. This can ensure detection of the final address in a page without using a counter circuit. It is therefore possible to simplify the structure of the final address detection circuit and reduce the circuit area occupying in a semiconductor memory device.

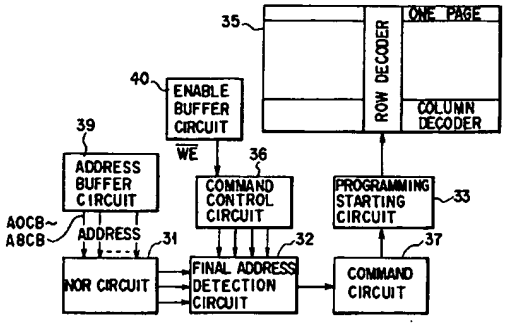

FIG. 3

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The present invention relates to a semiconductor memory device, for example, NAND type EEPROM (Electrically Erasable and Programmable ROM).

In this type of NAND EEPROM, data is basically written page by page. Since the page-by-page writing is done in such a way that programming is effected after all of one page of data is input to a latch circuit, the data input cycle should be discriminated from the program cycle. It is thus necessary to acknowledge the completion of input of the entire one page of data.

The end of the data input cycle is conventionally detected by counting the number of pieces of input data using a counter circuit.

Counter circuits conventionally used each occupy a large area in a semiconductor memory device and have a complicated structure.

It is therefore an object of the present invention to provide a semiconductor memory device which detects the final address in a page with a simple circuit occupying a smaller circuit area to be able to execute the next programming operation.

To achieve the foregoing object, a semiconductor memory device according to this invention comprises a non-volatile semiconductor memory element writable page by page, a detection circuit for detecting a final address in a page, and a write circuit for writing data into the non-volatile semiconductor memory element in accordance with an output signal of the detection circuit.

The detection circuit includes a plurality of NOR circuits for performing an NOR operation on an address bits by bits, and a NAND circuit for performing a NAND operation on an output signal of the NOR circuits.

According to this invention, when the detection circuit detects the final address in a page, the writing circuit writes data into the non-volatile semiconductor memory element. This structure ensures the detection of the final address in a page without using any counter circuit. It is thus possible to construct a final address detection circuit with a simple circuit and reduce the area of the circuit occupying in the semiconductor memory device.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a timing chart illustrating a page writing cycle of an EEPROM;

Fig. 2 is a diagram showing potentials applied when data of "0" is written in a memory cell;

Fig. 3 is a structural diagram illustrating one embodiment of the present invention;

Fig. 4 is a specific circuit diagram showing a NOR circuit shown in Fig. 3;

Fig. 5 is a specific circuit diagram showing a final address detection circuit shown in Fig. 3;

Fig. 6 is a specific circuit diagram showing a command control circuit shown in Fig. 3;

Fig. 7 is a specific circuit diagram showing a command circuit shown in Fig. 3;

Fig. 8 presents a timing chart illustrating the circuits shown in Figs. 4 to 7; and

Fig. 9 is a specific circuit diagram showing a program starting circuit shown in Fig. 3.

One preferred embodiment of the present invention will now be described referring to the accompanying drawings.

Fig. 1 illustrates a page writing cycle of an EEPROM.

The page writing cycle includes a command cycle, a data input cycle and a program cycle. In the command cycle a command for specifying the beginning of writing is fetched in response to single toggling of a WE (Write Enable) signal. By the next toggling of the WE signal, the data input cycle starts and input data is held as write data into a latch circuit connected to each bit line. When one page of data is all latched, the page writing cycle enters the program cycle to start running a program. The program cycle is a cycle with a relatively long period of execution as indicated by "t pH " in the diagram. In Fig. 1, after the program cycle comes a program verify cycle to verify the written data.

Fig. 2 illustrates potentials applied to a source 21, drain 22, well 23 and control gate 24 of a memory cell when data of "0" is written in that memory cell. With the potentials of the source 21, drain 22 and well 23 of the memory cell 20 set to 0 V and the potential of the control gate 24 set to Vpp (= 18 V), electrons are injected to the floating gate 25 by an F-N (Fowler-Nordheim) tunnel current.

Fig. 3 presents general circuit blocks according to one embodiment of the present invention. Individual address signals indicating an address in a page are supplied from an address buffer 39 to a NOR circuit 31 where they are NORed. The result of this operation is supplied as a final address detection signal to a final address detection circuit 32. This detection circuit 32 does not function in the data input cycle; it generates a signal only when the final address of a page is input. The output signal from the detection circuit 32 is supplied via a command circuit 37 to a program starting circuit 33. Upon reception of the output signal and after the rising of the WE signal, the program starting circuit 33 enables a row decoder 34 and a column decoder 38, both connected to a memory cell array 35, starting a program. Connected to the final address detection circuit 32 is a command control circuit 36 which controls the operation of

this circuit 32. Address buffer 39 outputs address signals A0CB to A8CB, while an enable buffer 40 outputs the write enable signal WE.

The command circuit 37 and program starting circuit 33 constitute a writing circuit that writes data into the semiconductor memory device 35.

Fig. 4 specifically illustrates the NOR circuit 31.

Referring to Fig. 4, "A0CB-A8CB" are inverted column address signals in a page column address. Those address signals A0CB-A8CB are supplied, three each, to 3-input NOR circuits 41, 42 and 43. Inverters 44, 45, 46, 47, 48 and 49 are connected, two each, to the output terminals of the NOR circuits 41, 42 and 43. For instance, when the address signals A0, A1 and A2 are at a high level, their inverted address signals A0CB, A1CB and A2CB become a low level, setting the output of the NOR circuit 41 to a high level. Eventually, a high-level final address detection signal CLAST3 will be output from the output terminal of the inverter 45. The same is true of the inverted address signals A3CB to A8CB. When the inverted address signals A3CB, A4CB and A5CB are at a low level, a high-level final address detection signal CLAST2 will be output from the output terminal of the inverter 47; and when the inverted address signals A6CB, A7CB and A8CB are at a low level, a high-level final address detection signal CLAST1 will be output from the output terminal of the inverter 49.

As an input consists of 512 bytes in this embodiment, the number of address lines is set to nine. Even if the number of input addresses or the page length changes, a similar circuit can be used. The final address detection signals CLAST1, CLAST2 and CLAST3 do not become a high level unless the final address is input or all the column page addresses are a high level.

Fig. 5 illustrates the final address detection circuit 32.

This detection circuit 32 comprises a 3-input NAND circuit 51, a NOR circuit 52, two latch circuits 53 and 54, and inverter 55. Each of the latch circuits 53 or 54 includes two inverters 53a and 53b (54a and 54b), two transfer gates 53c and 53d (54c and 54d), and an N channel MOSFET 53e (54e).

The final address detection signals CLAST1, CLAST2 and CLAST3 are supplied to the NAND circuit 51. The output signal of the NAND circuit 51 is supplied to one input terminal of the NOR circuit 52. The other input terminal of the data NOR circuit 52 and the gates of the N channel MOSFETs 53e and 54e are supplied with a RESET signal. The transfer gates 53c and 54d are respectively supplied with a command control signal WES1 and an inverted command control signal WES1B, while the transfer gates 53d and 54c are respectively supplied with a command control signal WES2 and an inverted command control signal WES2B.

Fig. 6 illustrates the command control circuit 36. This control circuit 36, which generates the mentioned command control signals WES1, WES1B, WES2 and WES2B, comprises NAND circuits 60 and 61, NOR circuits 62 and 63, and inverters 64 to 69, for example. The command control circuit 36 generates the command control signals WES1, WES1B, WES2 and WES2B shown in Fig. 8 in response to the toggling of the WE signal (WES).

In Fig. 5, when the final address detection signals CLAST1, CLAST2 and CLAST3 are all at a high level, a low-level signal is output from the output terminal of the NAND circuit 51. This low-level signal is transferred in order to the latch circuits 53 and 54 in accordance with the cycles of the command control signals WES1, WES1B, WES2 and WES2B, and a CLASTB signal indicating that the final address has been input is output from the output terminal of the inverter 55. This CLASTB signal is input to the command circuit 37. Signals at individual notes N1 to N5 of the final address detection circuit 32 are shown in Fig. 8.

Fig. 7 illustrates the command circuit 37.

The command circuit 37 comprises an 3-input NOR circuit 71, two latch circuits 72 and 73, and inverters 74 to 77. Each of the latch circuits 72 or 74 includes two inverters 72a and 72b (73a and 73b), two transfer gates 72c and 72d (73c and 73d), and an N channel MOSFET 72e (73e).

The CLASTB signal is supplied together with a program mode signal CMDLB and the RESET signal to the NOR circuit 71. The output signal of this NOR circuit 71 is supplied to the latch circuit 72. The program mode signal CMDLB is acquired by decoding a signal given from a Din pin. The signal CMDLB indicates that a write command fetched in the command cycle is accepted, which means that the memory cell is in data input mode. The transfer gates 72c and 73d are respectively supplied with the command control signal WES2 and the inverted command control signal WES2B, while the transfer gates 72d and 73c are respectively supplied with the command control signal WES1 and the inverted command control signal WES1B. The gates of the N channel MOSFETs 72e and 73e are supplied with the RESET signal.

When the CLASTB signal is supplied to the NOR circuit 71, this signal is transferred to the latch circuits 72 and 73 and the inverters 74 to 77 in order, and is output as a CRPO from the output terminal of the inverter 77.

Upon reception of the CRPO signal, the program starting circuit 33 applies a potential necessary for a program to the control gate of the memory cell. In writing data, the potential applied to the control gate is Vpp.

Fig. 9 illustrates the program starting circuit 33.

In the program starting circuit 33 that applies the potential Vpp, the CRPO signal is connected to the gates of a P channel MOSFET 923 and an N channel MOSFET 93. The MOSFET 92 has its source and back gate connected via a depletion type N channel MOSFET 91 to a power supply VppRW. The drain of the MOSFET 92 is connected via a depletion type N channel MOSFET 99 to the drain of the MOSFET 93. The source of the MOSFET is grounded. The drain of the MOSFET 92 is connected to the gates of depletion type N channel MOSFETs 94 and 96 as well as to the gate of the N channel MOSFET 91. The MOSFET 94 has a drain connected to the power supply VppRW, and its source is connected to the source and back gate of a P channel MOSFET 95. The MOSFET 95 has a gate connected to the gate of the N channel MOSFET 93, and a drain connected to the drain of the depletion type N channel MOSFET 96. The source of this MOSFET 96 is connected to the control gate CG of the memory cell (not shown).

When the CPRO signal corresponding to the final address detection signals is supplied to the program starting circuit 33 having the above structure, the MOSFETs 92 and 95 are turned on and the MOSFET 93 is turned off. Until the MOSFET 92 is turned on, the potential of a node 98 is 0 V and the MOSFET 91 sends a potential for the threshold value to a node 97. Thereafter, through this loop, the potential of the node 98 is raised to the power supply potential Vpp. Consequently, the MOSFETs 94 and 96 are turned on, applying the potential Vpp to the control gate CG of the memory cell.

According to this embodiment, a plurality of NOR circuits perform a NOR operation on the address bits by bits, and send their output signals CLSST1, CLAST2 and CLAST3 to the NAND circuit 51 of the final address detection circuit 32, thereby producing the signal CLASTB that indicates the final address. Since this design, unlike the prior art, eliminates the need for a complex and large counter circuit, it is possible to simplify the structure of the final address detection circuit and reduce the circuit area occupying in the semiconductor memory device.

The present invention is not limited to this embodiment, but may be modified in various manners within the scope and spirit of the invention.

As described above, the present invention can provide a semiconductor memory device which detects the final address in a page with a simple circuit occupying a smaller circuit area to be able to execute the next programming operation.

Claims

1. A semiconductor memory device comprising:
   a non-volatile semiconductor memory device (35) writable page by page;
   a final address detection circuit (32) for detecting a final address in a page; and
   a write circuit (33, 37) for writing data into said non-volatile semiconductor memory device (35) in accordance with an output signal of said final address detection circuit (32).

2. A semiconductor memory device comprising:
   a non-volatile semiconductor memory device (35) writable page by page;
   a NOR circuit (31) for performing a NOR operation on an address signal from an address buffer (39) and outputting a final address detection signals for detecting a final address of a page of said non-volatile semiconductor memory device (35);
   a final address detection circuit (32) for receiving said final address detection signals from said NOR circuit (31) to detect said final address in said page; and
   a write circuit (33, 37) for writing data into said non-volatile semiconductor memory device (35) in accordance with an output signal of said final address detection circuit (32).

3. The semiconductor memory device according to claim 2, characterized in that said detection circuit includes a plurality of NOR circuits for performing an NOR operation on an address bits by bits, and a NAND circuit for performing a NAND operation on an output signal of said NOR circuits.

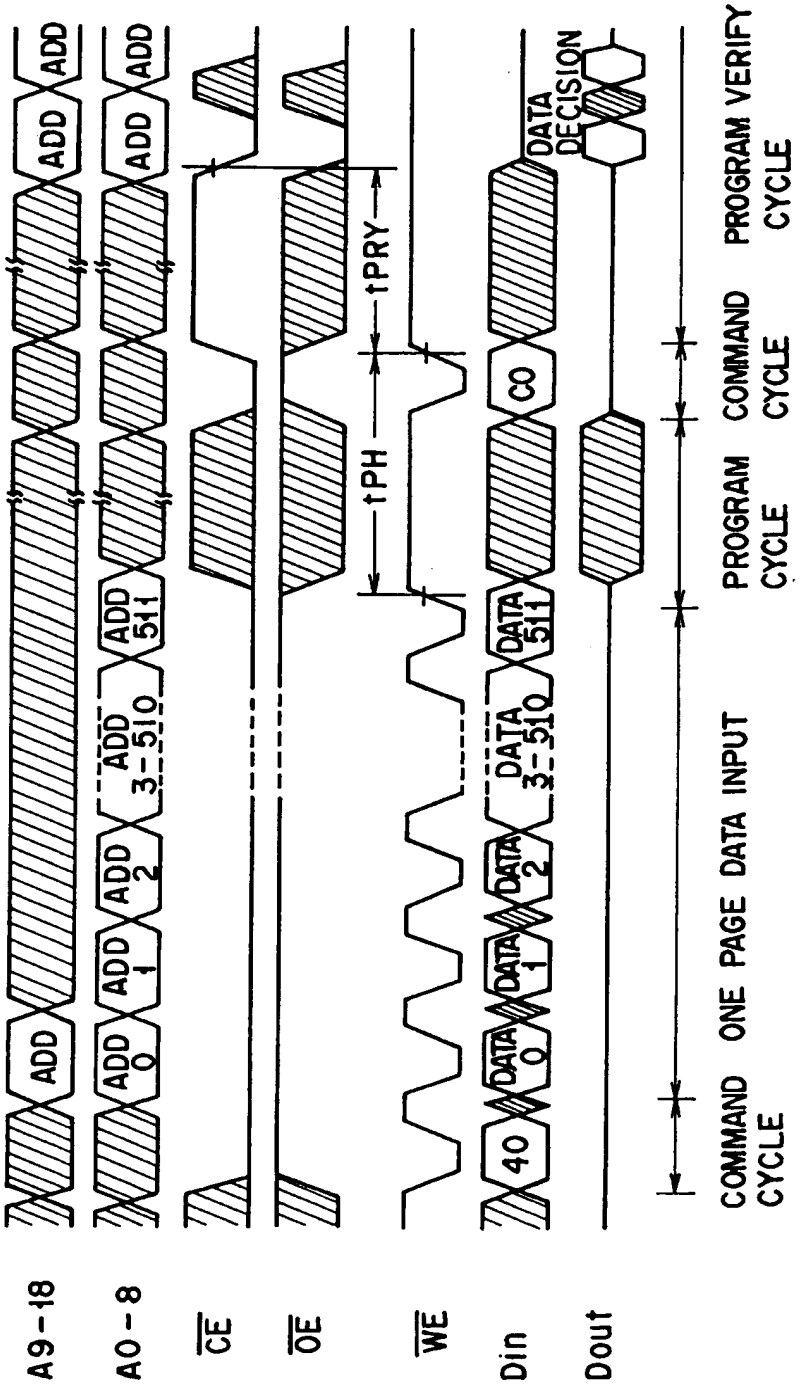

A9-18
A0-8
CE
OE
WE
Din
Dout
ADD
ADD 0
ADD 1
ADD 2
ADD 3-510
ADD 511
40
DATA 0
DATA 1
DATA 2
DATA 3-510
DATA 511
C0
DATA DECISION
tPH
tPRY
COMMAND CYCLE
ONE PAGE DATA INPUT
PROGRAM CYCLE
COMMAND CYCLE
PROGRAM VERIFY CYCLE

FIG. 1

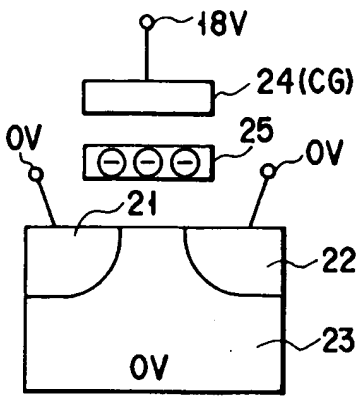


FIG. 2

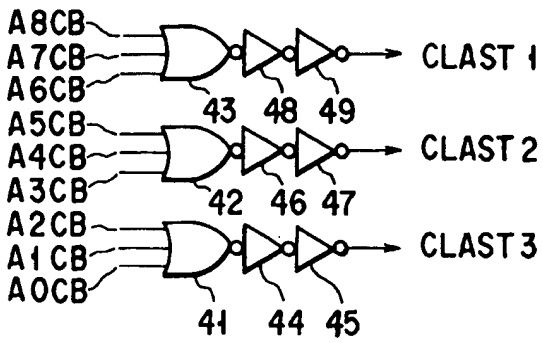


FIG. 4

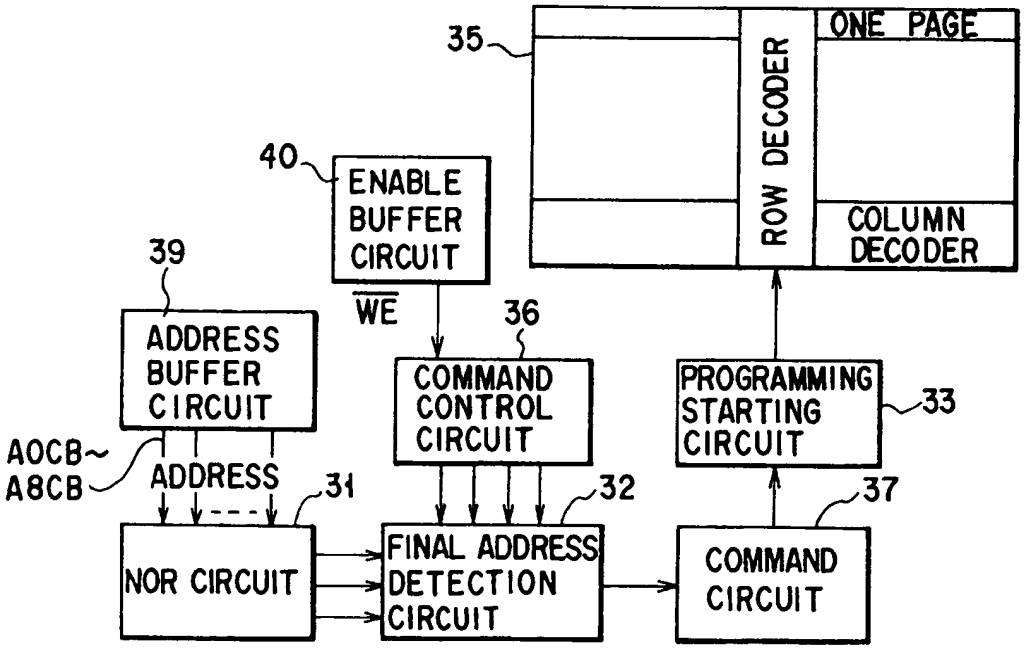


FIG. 3

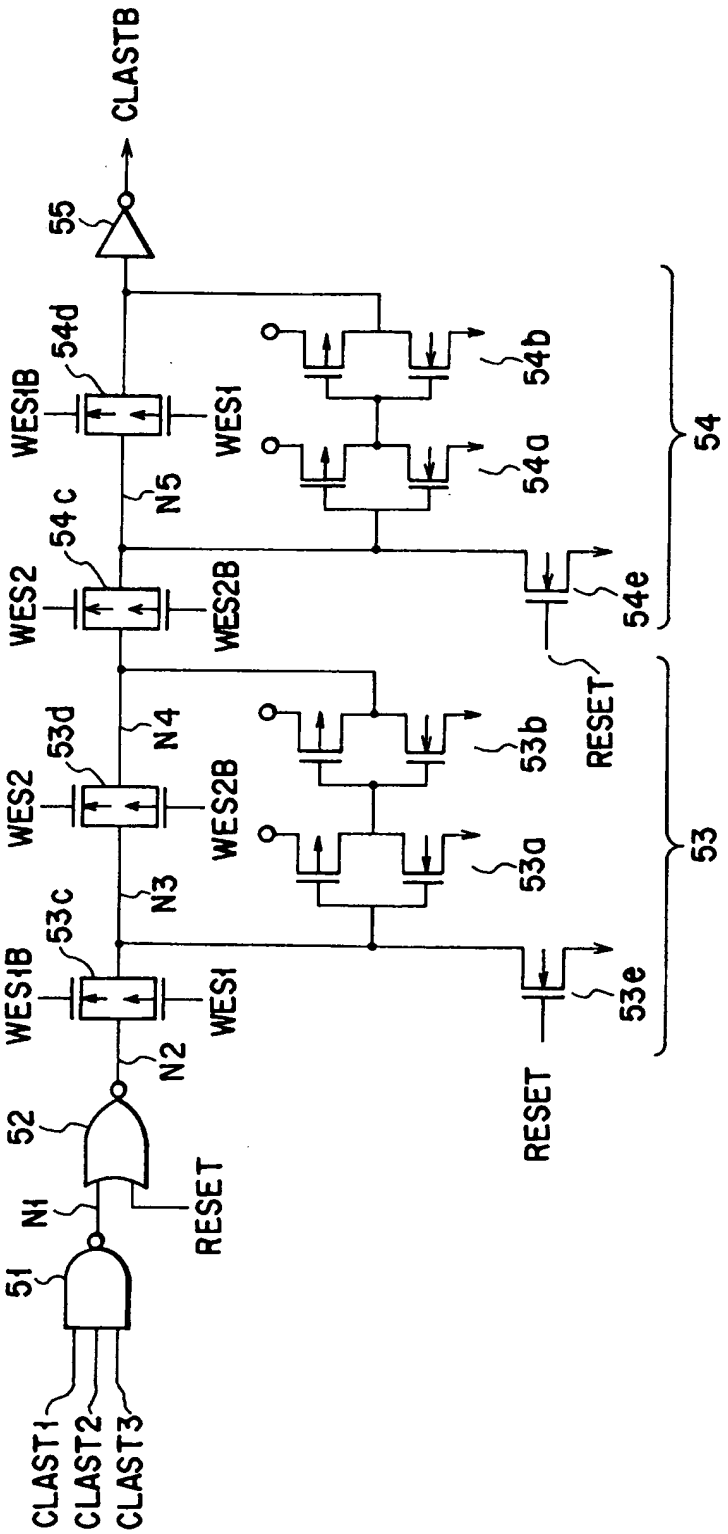

CLAST1
CLAST2
CLAST3
51
N1
52
RESET
N2
WES1B
WES1
53c
N3
WES2
WES2B
53d
N4
WES1B
WES1
54d
N5
WES2
WES2B
54c
RESET
53a
53b
53e
RESET
54a
54b
54e
53
54
55
CLASTB

FIG. 5

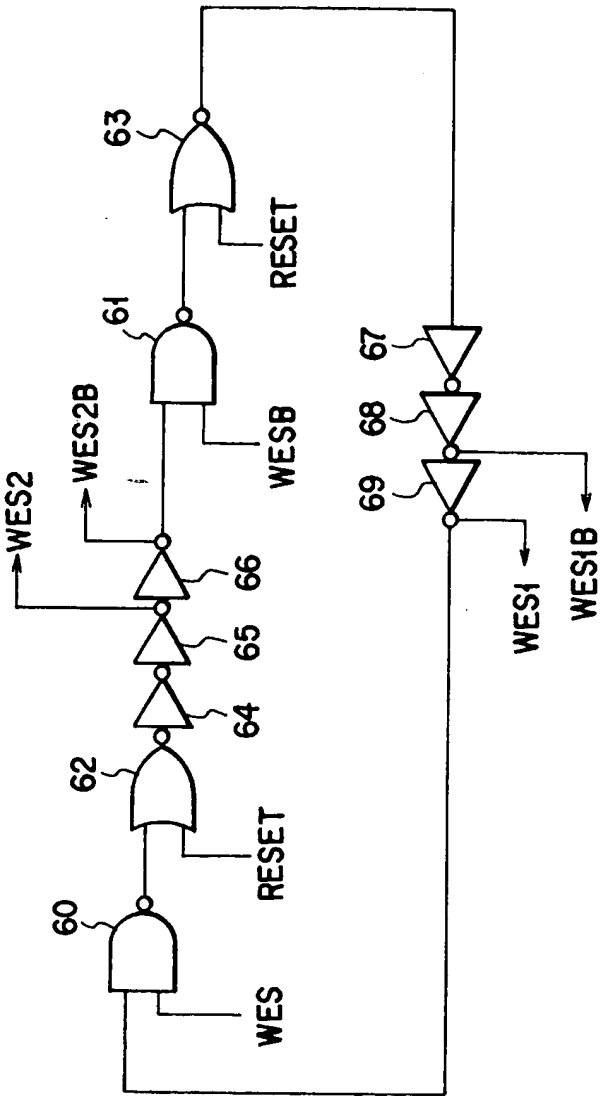

63
RESET
61
WES2B
WES2
WESB
66
65
64
62
RESET
60
WES
67
68
69
WES1
WES1B

FIG. 6

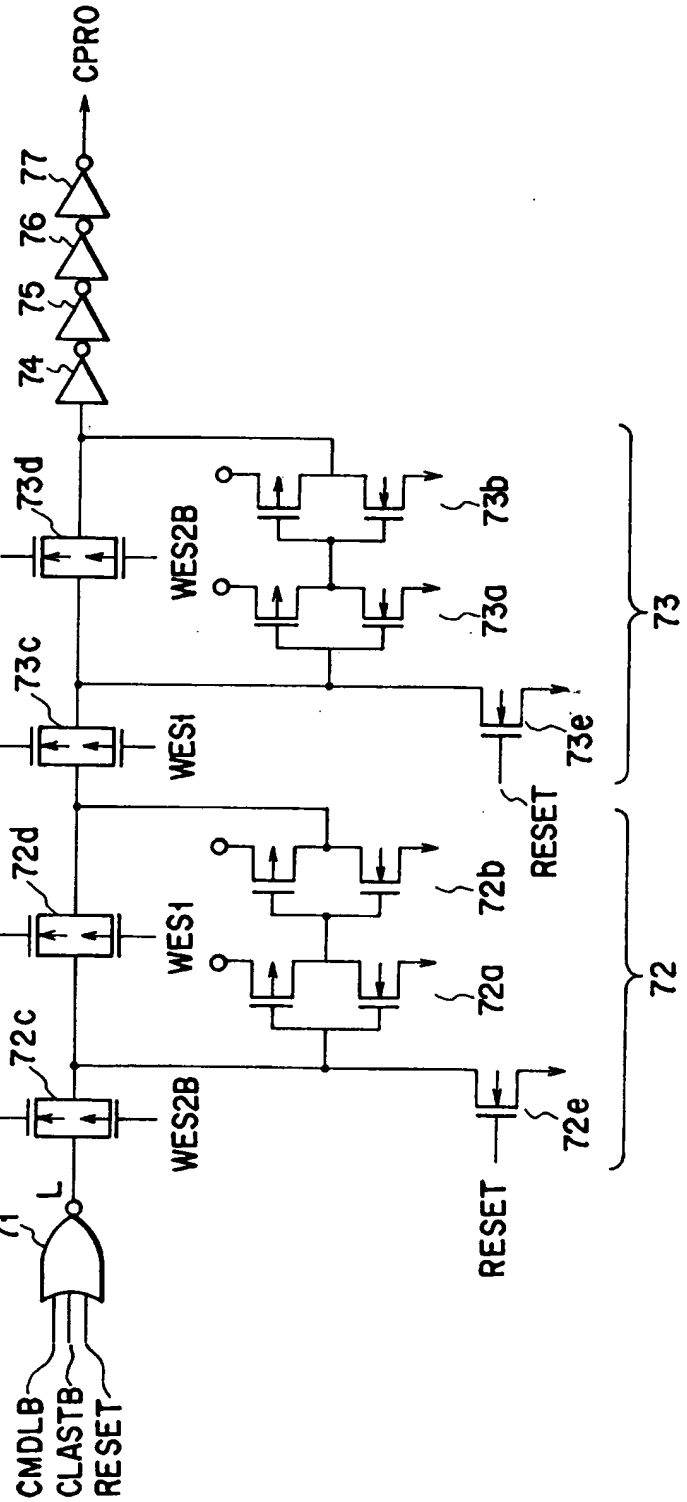
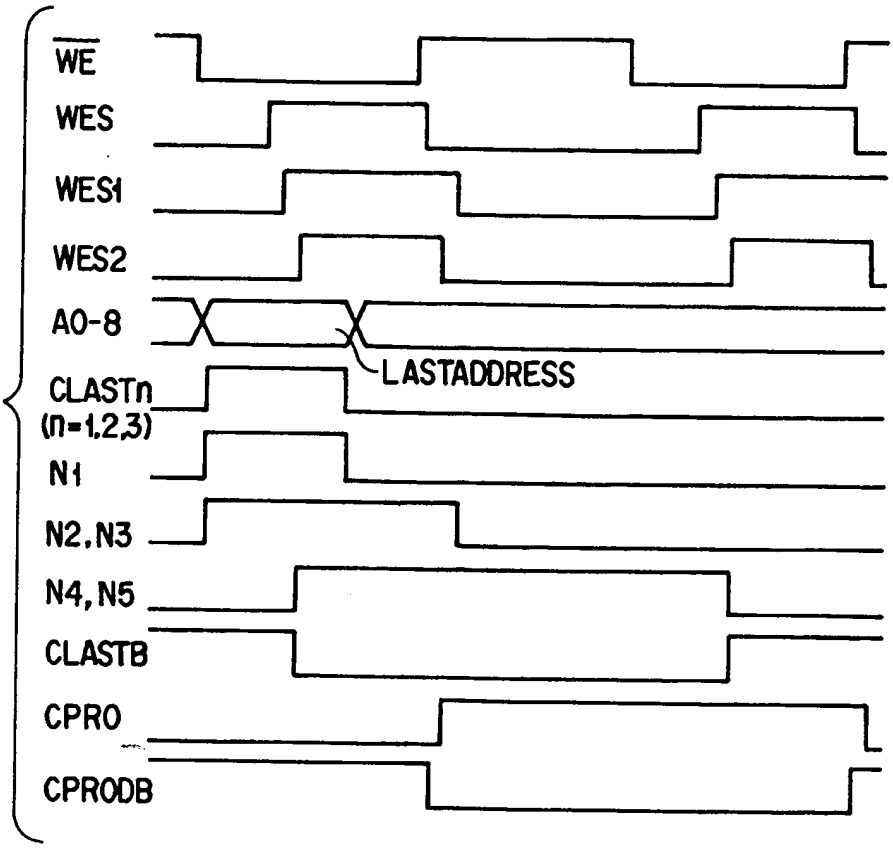

CPRO
77
76
75
74
WES2
73d
WES2B
73b
73a
WES1B
73c
WES1
73e
73
RESET
WES1B
72d
WES1
72b
72a
WES2
72c
WES2B
72e
72
RESET
L
71
CMDLB
CLASTB
RESET

FIG. 7

FIG. 8


WE
WES
WES1
WES2
A0-8
LASTADDRESS
CLASTn
(n=1,2,3)
N1
N2, N3
N4, N5
CLASTB
CPRO
CPRODB

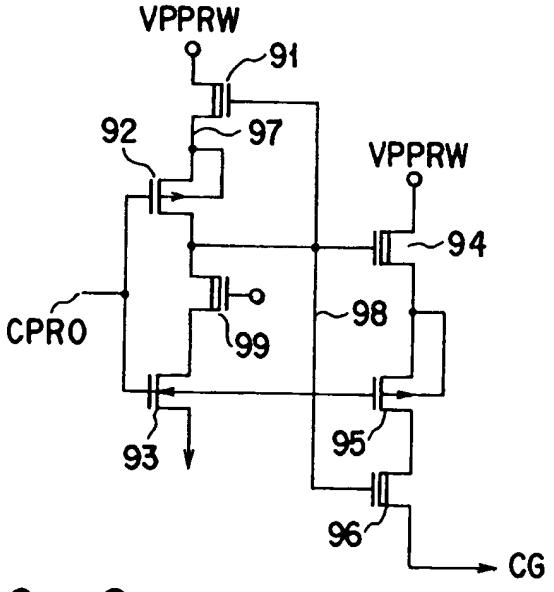

VPPRW
91
92
97
VPPRW
94
CPRO
98
99
93
95
96
CG

FIG. 9